Appl. No. 10/521,260
Amendment and/or Response
Reply to Office action of 21 March 2007

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Amendments to the Claims:

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) A method of determining the values of data bits from a demodulated frequency shift key signal, comprising over-sampling raw data recovered from the demodulated signal, delaying samples of the raw data, combining selected delayed samples of the raw data to form a sample to be bit sliced, bit slicing the samples to be sliced to produce a bit stream signal, delaying the bit stream signal, using the bit stream signal to recover a clock signal, and using the recovered clock signal to sample the delayed bit stream signal at the data rate to produce detected bits.

2. (Currently Amended) A method as claimed in claim 1, ~~characterised in that~~wherein samples of the delayed raw data occurring after ~~a~~delays of substantially half a bit period, and one and a half bit periods, are combined to form samples to be bit sliced.

3. (Currently Amended) A method as claimed in claim 1, ~~characterised in that~~wherein at least two successive samples of the raw data occurring after a delay of substantially half a bit period are added and multiplied by a gain factor and the result is added to at least one sample of raw data occurring after a delay of substantially one and a half bit periods.

4. (Currently Amended) A method as claimed in claim 3, ~~characterised in that~~wherein the gain factor has a value of ~~substantially~~substantial unity.

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5. (Currently Amended) A method as claimed in any one of claims 1 to 4, ~~characterised by~~further comprising normalising the sample to be sliced prior to bit slicing.

6. (Currently Amended) A receiver for use with FSK signals, comprising:

_____a demodulator ~~(14)~~ for demodulating an FSK signal, oversampling the demodulated FSK signal with an oversampling ratio, N, and supplying over-sampled raw data,

_____first delay means ~~(60)~~ for delaying the over-sampled raw data,

_____means ~~(66, 68, 70)~~ for combining selected delayed samples of the raw data to provide samples to be sliced,

_____bit slicing means ~~(22)~~ for producing a bit stream signal from the samples to be sliced,

_____second delay means ~~(30, 32)~~ for delaying the bit stream signal,

_____clock recovery means (74) coupled to the bit slicing means[[,]] ~~(22)~~ and

_____bit sampling means coupled to an output of the second delay means ~~(30, 32)~~ and controllable by the clock recovery means ~~(74)~~ to produce detected bits.

7. (Currently Amended) A receiver as claimed in claim 6, ~~characterised in that~~wherein the first delay means ~~(60)~~ comprises shift register means having at least ~~3N/2~~(3N/2 -1) stages, ~~where N is the number of stages corresponding to the over-sampling ratio,~~ and ~~in that~~wherein outputs from~~, or in the vicinity of,~~ stages ~~N/2~~ in a range of (N/2 ± 1) and ~~3N/2~~ in a range of (3N/2 ± 1) are applied to the combining means ~~(66, 68, 70)~~.

8. (Currently Amended) A receiver as claimed in claim 6, ~~characterised in that~~wherein the first delay means ~~(60)~~ comprises shift register means having 3N/2 stages, ~~where N is the number of stages corresponding to the over-sampling ratio,~~ and ~~in that~~wherein the combining means ~~(66, 68, 70)~~ comprises a first adding stage coupled to outputs of two adjacent shift register stages in ~~the vicinity of stage N/2~~a

range of (N/2 ± 1), a scaling stage coupled to an output of the first adding stage, a second adding stage having a first input coupled to an output of the scaling stage, a second input coupled to output of a shift register ~~at, or in the vicinity of, the stage~~ ~~3N/2~~in a range (3N/2 ± 1) and an output coupled to the bit slicing means ~~(22)~~.

9. (Currently Amended) A receiver as claimed in claim 8, ~~characterised in~~ ~~that~~wherein the scaling stage has a scaling factor of ~~substantially~~ substantial unity.

10. (Currently Amended) A receiver as claimed in claim 7, 8 or 9, ~~characterised in that~~wherein the over-sampling ratio equals 20, ~~in that~~wherein outputs of stages 9, 10 and 29 are applied to the combining means ~~(66, 68, 70)~~.

11. (Currently Amended) A receiver as claimed in any one of claims 6 to 10, ~~characterised in that~~wherein the second delay means ~~(30, 32)~~ comprises first and second delay stages, each having a delay of substantially one bit period, in that the bit slicing means has means for storing a plurality of threshold values, and means for selecting a threshold value for comparison with the currently held samples to be sliced in dependence on the bit values at outputs of the first and second delay stages.

12. (New) The method of claim 3, wherein the gain factor is in a range from 0.8 to 1.0.

13. (New) The receiver of claim 3, wherein the scaling stage has a scaling factor in a range from 0.8 to 1.0.